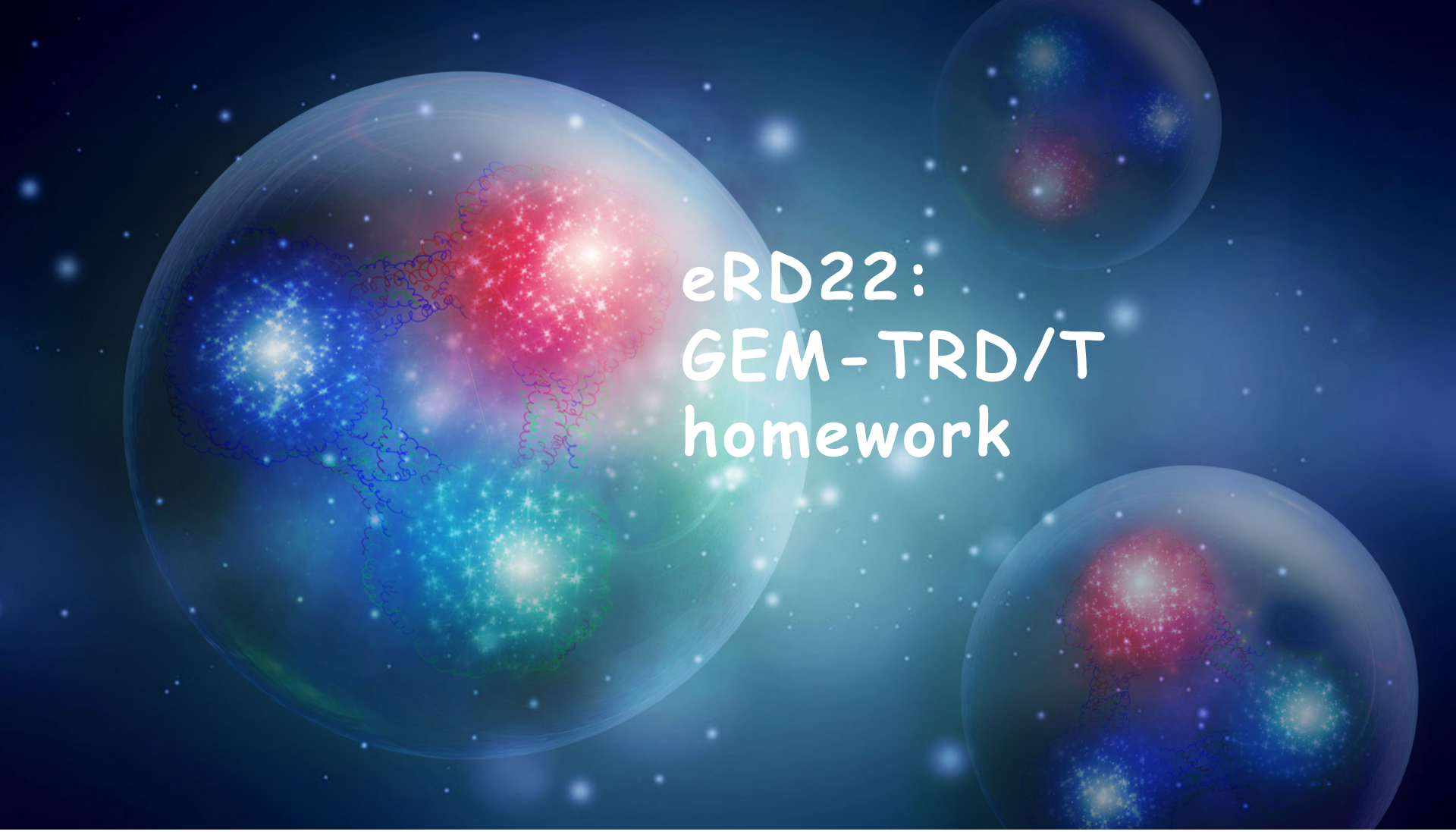


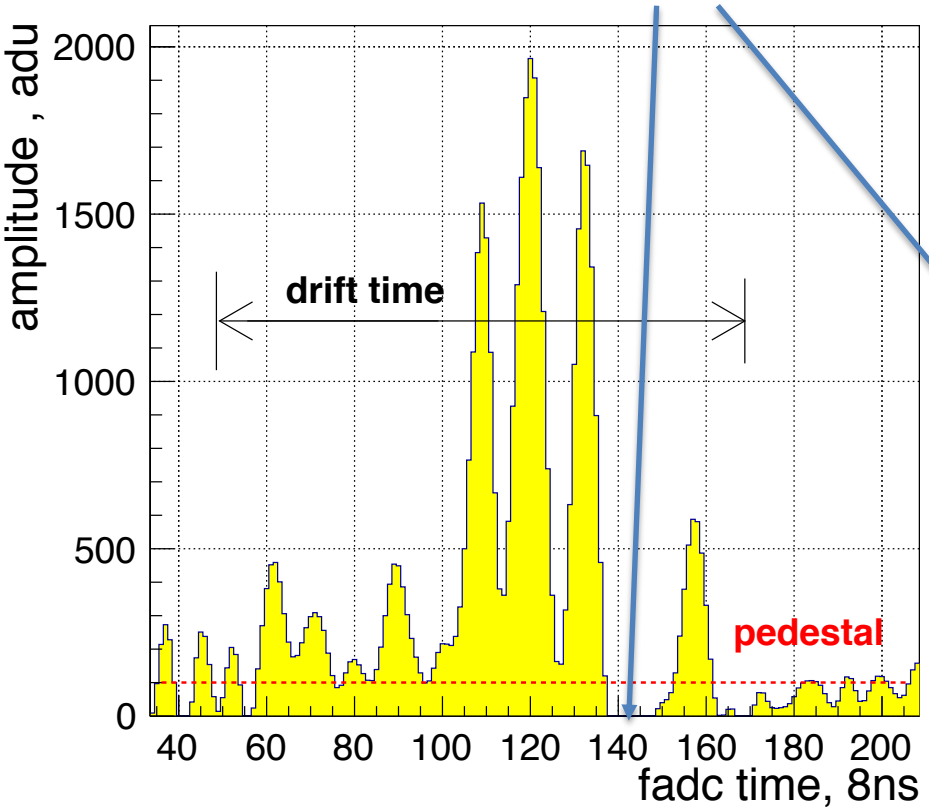
Yulia Furletova (JLAB) on behalf of GEM-TRD/T working group

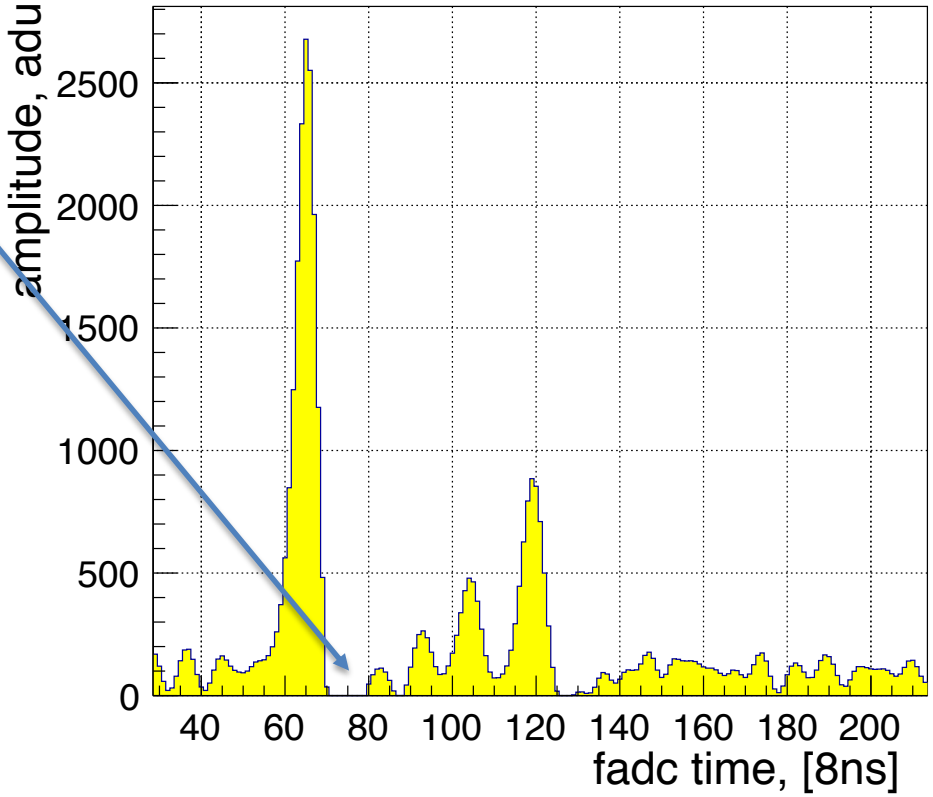
1) “Please explain the non-negotiable specifications for the electronics for a realistic test of the TRD. For example, what is the requirement for the peaking time? Suggest your solution.”

- ✓ FlashADC 125MHz (8ns/bin) 12bit ADC (currently have) : perfect!
- ✓ Minimum: 80MHz and 10bit ADC (?) need to do simulation (by adding bins from FlashADC)

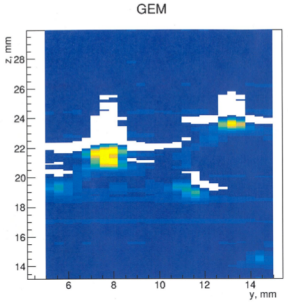
Problem: Pre-amp (GAS-II chip) can live with it for now, but would like to improve!

base-to-base time 10bins (x8ns) = 80ns (ok), but undershooting (no base-line restorers) => loosing clusters!





Readout electronics



"1) Please explain the non-negotiable specifications for the electronics for a realistic test of the TRD. For example, what is
the requirement for the peaking time?
Suggest your solution."

Solution:

- Problem with current setup (with GAS-II chips) only seen if we use cluster counting method (we are loosing clusters!).
- for the average dE/dx (where we compare energy per bin) we could relax requirements for timing (MHz) from 125MHz to ~80 MHz…

- FlashADC and our current setup: this is for test purpose only, once we understand which way is better to go (or for mass-production) we might revise our requirements.

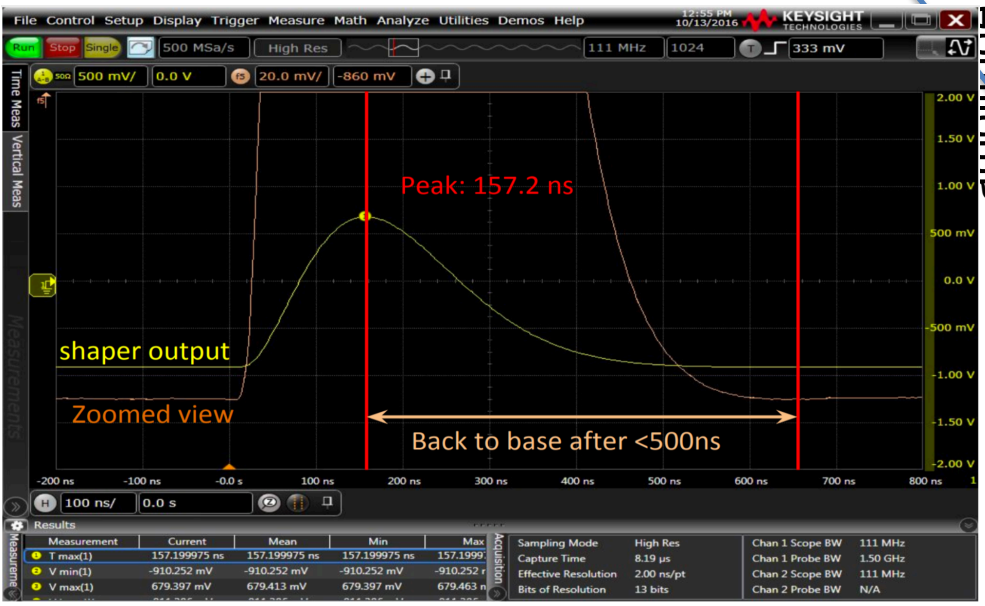
- For Fermilab/ CERN testbeams:

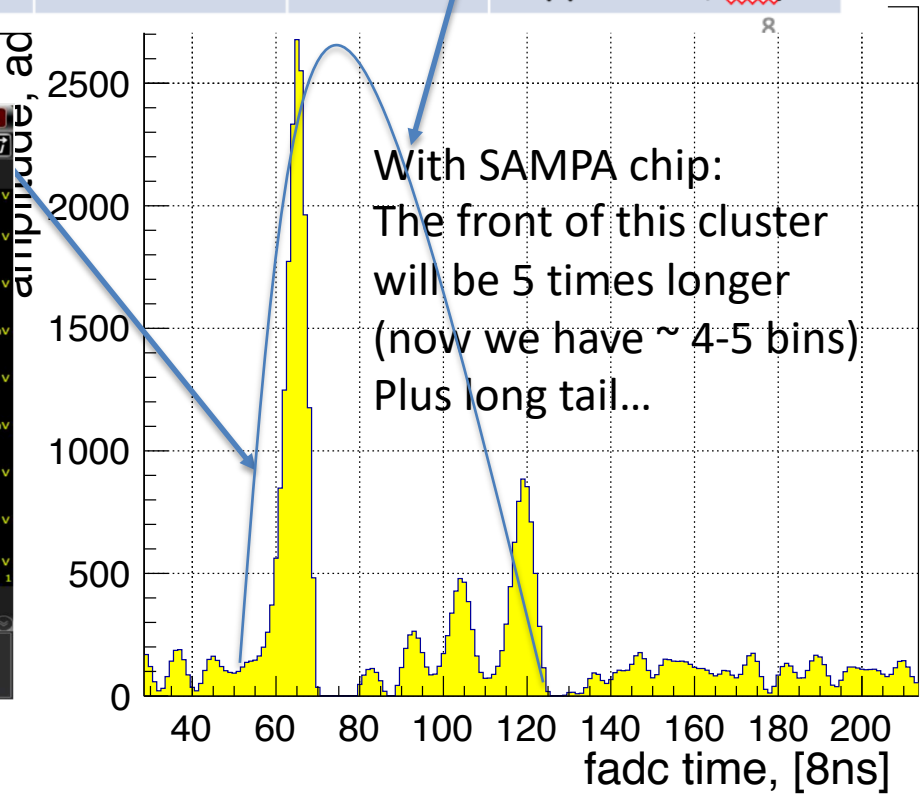
1) Currently discussing with JLAB electronic department for "portable" FlashADCs" (and , if possible, improve GAS-II preamp).
2) An other idea is to borrow and test with SAMPA chips from BNL (???).
3) Also we had discussions over coffee with Mickey Chiu (and Jin) , an other solution with DRS4 test board … need to look at specifications… looks too good at first glance ! ;-)

1) “Please explain the non-negotiable specifications for the electronics for a realistic test of the TRD. For example, what is the requirement for the peaking time? Suggest your solution.”

	MHz	ns/bin	Peaking time	Range	Channels/chip cost	ADC bits	Shaper
SAMPA (ALICE)	10-20	100-50	160ns	Stream 3.2Gbit/s	32chan/chip 30$/chip 1$/channel	10bit	500ns- return to baseline Baseline restorer, DSP (zero-suppression, thr)

ALICE TPC upgrade and the SAMPA ASIC

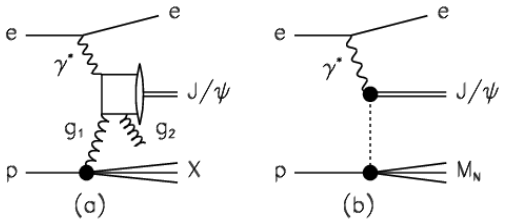


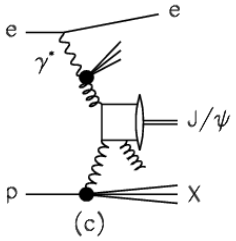


2) “How does the lack of electronics limit the tests?”

- For the current setup at JLAB : no limitations
- For away test beams (e/π) Fermilab/CERN: need our own, preferably with performance the same (or close) as we currently have.
- and capable to operate in streaming mode (for final EIC setup)

Electron/hadron separation





3) A more general questions:
"What software tools are currently missing and impede your progress in the detector development effort?"

We have all software in hands (GEANT4, GARFIELD, etc) for the standalone detector developments!

But …
We would like to understand an impact of our detector for other (or with other) subdetectors:

- Benefit for DRICH, EMCAL (tracking)
- Global PID (e/π)
- Having an ability to change a configuration of EIC detector and see effect of TRD for physics analysis (J/Psi, Heavy-quarks, etc)

Backup